[Name of the Document] Abstract

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[Problem] To reduce the area of each ferroelectric memory cell.

[Solution] Plate lines **101a** through **101d** run in the word line direction above ferroelectric capacitors of ferroelectric memory cells **108** adjacent to each other in the word line direction. Bit line contacts **107** are placed in regions between the plate lines **101a** through **101d** adjacent to each other in the bit line direction and between storage nodes **104a** through **104d** of the ferroelectric capacitors adjacent to each other in the word line direction. Cut portions are formed at positions of the plate lines **101a** through **101d** near the bit line contacts **107**. Active regions **106** of transistors extend so as to intersect with the word line direction and the bit line direction.

[Selected Figure] FIG. **1**